Amendments to the Claims:

Please amend claims 27, 36, 72, 73 and 87 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1.-26. (Cancelled)

27. (Currently Amended) A MOS transistor having elevated source and drain structures, comprising:

a gate dielectric layer on a substrate;

a gate electrode on the gate dielectric layer;

an epitaxial layer contacting ~~a~~ side portions of the gate dielectric layer on the substrate and extending from the gate dielectric layer substantially parallel to the substrate in a horizontal direction ~~substantially parallel to the substrate~~;

first source/drain regions in the epitaxial layer contacting the side portions of the gate dielectric layer at lower side portions of the gate electrode; and

insulating sidewall spacers ~~having bottom portions~~ on the first source/drain regions in the epitaxial layer at ~~an~~ upper side portions of the gate electrode, bottom surfaces of the insulating sidewall spacers extending from the upper side portions of the gate electrode substantially parallel to the substrate.

28. (Previously Presented) The transistor of claim 27, wherein the gate dielectric layer extends across a bottom portion and the lower side portions of the gate electrode;

29. (Previously Presented) The transistor of claim 27, wherein the first source/drain regions are formed by doping the epitaxial layer with impurities.

30. (Previously Presented) The transistor of claim 27, further comprising second

source/drain regions adjacent the first source/drain regions opposite the gate electrode.

31 (Previously Presented) The transistor of claim 30, wherein the second source/drain regions are formed by doping exposed surfaces with impurities using the gate electrode and insulating sidewall spacers as masks.

32. (Previously Presented) The transistor of claim 30, wherein the first source/drain regions comprise source/drain extension regions and wherein the second source/drain regions comprise deep source/drain regions.

33. (Previously Presented) The transistor of claim 30, wherein depths of the first source/drain regions are less than depths of the second source/drain regions.

34. (Previously Presented) The transistor of claim 30, wherein the second source/drain regions extend into portions of the substrate.

35. (Previously Presented) The transistor of claim 29, wherein the first source/drain regions extend into portions of the substrate.

36. (Currently Amended) The transistor of claim 27, wherein the substrate is formed using one selected from the group consisting of silicon[[;]], silicon-on-insulator (SOI), SiGe[[;]], SiGe-on-insulator(SGOI), strained silicon, strained silicon-on-insulator, and GaAs.

37. (Previously Presented) The transistor of claim 27, wherein the epitaxial layer comprises silicon or silicon germanium.

38 (Previously Presented) The transistor of claim 27, wherein the gate dielectric layer and gate electrode extend into a trench formed in an upper portion of the substrate.

39. (Previously Presented) The transistor of claim 38, wherein the trench is of a depth that is

less than about 50nm.

40. (Previously Presented) The transistor of claim 27, further comprising a channel region in the substrate under the gate electrode and adjacent the lower side portions of the gate electrode.

41. (Previously Presented) The transistor of claim 27, wherein the gate dielectric layer comprises a material selected from the group of materials consisting of silicon oxide, silicon oxy-nitride (SiON), tantalum oxide, and a high-dielectric-constant material.

42. (Previously Presented) The transistor of claim 27, wherein the gate dielectric layer is formed using a deposition process or a thermal oxidation process.

43. (Previously Presented) The transistor of claim 27, wherein the gate electrode comprises a film selected from the group of materials consisting of a polysilicon film, a silicon geranium film, a silicide film, a metal film, and a laminate film.

44. (Previously Presented) The transistor of claim 27, further comprising a silicon oxide buffer layer between the gate electrode and the insulating sidewall spacers.

45. (Previously Presented) The transistor of claim 27, further comprising a silicide film on the first source/drain regions and the gate electrode.

46. (Previously Presented) The transistor of claim 45, wherein the silicide film comprises a material selected from the group consisting of Co, Ni, W, Ti and combinations thereof.

47.-71. (Cancelled)

72. (Currently Amended) A MOS transistor having elevated source and drain structures, comprising:

a gate dielectric layer on a substrate;

a gate electrode on the gate dielectric layer, wherein the gate dielectric layer includes a horizontal portion that extends across a bottom portion of the gate electrode and side~~vertical~~ portions that extend in a vertical direction along lower side portions of the gate electrode;

an epitaxial layer contacting ~~a~~ the side portions of the gate dielectric layer on the substrate and extending from the ~~vertical~~side portions of the gate dielectric layer substantially parallel to the substrate in a horizontal direction ~~substantially parallel to the substrate~~; and

first source/drain regions in the epitaxial layer contacting side portions of the gate dielectric layer at the lower side portions of the gate electrode.

73. (Currently Amended) The transistor of claim 72, further comprising insulating sidewall spacers on the epitaxial layer at ~~an~~ upper side portions of the gate electrode.

74. (Cancelled)

75. (Previously Presented) The transistor of claim 72, wherein the first source/drain regions are formed by doping the epitaxial layer with impurities.

76. (Previously Presented) The transistor of claim 72, further comprising second source/drain regions adjacent the first source/drain regions opposite the gate electrode .

77. (Previously Presented) The transistor of claim 76, wherein the second source/drain regions are formed by doping exposed surfaces with impurities using the gate electrode and insulating sidewall spacers as masks.

78. (Previously Presented) The transistor of claim 76, wherein the first source/drain regions comprise source/drain extension regions and wherein the second source/drain regions comprise

deep source/drain regions.

79. (Previously Presented) The transistor of claim 76, wherein depths of the first source/drain regions are less than depths of the second source/drain regions.

80. (Previously Presented) The transistor of claim 76, wherein the second source/drain regions extend into portions of the substrate.

81. (Previously Presented) The transistor of claim 76, wherein the first source/drain regions extend into portions of the substrate.

82. (Previously Presented) The transistor of claim 72, wherein the substrate is formed using one selected from the group consisting of: silicon, silicon-on-insulator (SOI), SiGe, SiGe-on-insulator(SGOI), strained silicon, strained silicon-on-insulator, and GaAs.

83. (Previously Presented) The transistor of claim 72, wherein the epitaxial layer comprises silicon or silicon germanium.

84. (Previously Presented) The transistor of claim 72, wherein the gate dielectric layer and gate electrode extend into a trench formed in an upper portion of the substrate.

85. (Previously Presented) The transistor of claim 84, wherein the trench is of a depth that is less than about 50nm.

86. (Previously Presented) The transistor of claim 72, further comprising a channel region in the substrate under the gate electrode and adjacent the lower side portions of the gate electrode.

87. (Currently Amended) The transistor of claim 72, wherein the gate dielectric layer comprises a material selected from the group consisting of[[,]]: silicon oxide, silicon oxy-nitride (SiON), tantalum oxide, and a high-dielectric-constant material.

88. (Previously Presented) The transistor of claim 72, wherein the gate dielectric layer is formed using a deposition process or a thermal oxidation process.

89. (Previously Presented) The transistor of claim 72 wherein the gate electrode comprises a film selected from the group consisting of a polysilicon film, a silicon geranium film, a silicide film, a metal film, and a laminate film.

90. (Previously Presented) The transistor of claim 72, further comprising a silicon oxide buffer layer between the gate electrode and the insulating sidewall spacers.

91. (Previously Presented) The transistor of claim 72, further comprising a silicide film on the first source/drain regions and the gate electrode.

92. (Previously Presented) The transistor of claim 91, wherein the silicide film comprises a material selected from the group consisting of Co, Ni, W, Ti and combinations thereof.

93. (Previously Presented) The transistor of claim 72, wherein the gate dielectric layer and the gate electrode are formed following formation of the epitaxial layer.

94. (Previously Presented) The transistor of claim 72, wherein the gate dielectric layer and the gate electrode are formed in an opening between neighboring portions of the epitaxial layer, the opening exposing the substrate.

95. (Previously Presented) The transistor of claim 27 wherein the first source/drain regions are formed before formation of the sidewall spacers.